REMARKS

Claims 1-29 are previously pending.

Claims 1-6, 8-17, 19-23 and 27 are rejected under 35 USC §102(e) as anticipated by Agarwal et al. (U.S. Pub. No. 2002/0037630).

Claims 7, 18, 24 and 25 are rejected under 35 USC §103(a) as being unpatentable over Agarwal '630 in view of Aoki et al. (U.S. Patent No. 6,303,950).

Claim 26 is rejected under 35 USC §103(a) as being unpatentable over Agarwal '630.

Claims 28 and 29 are rejected under 35 USC §103(a) as being unpatentable over Agarwal '630 in view of Narwanka et al. (U.S. Patent No. 6,204,203).

The Applicant amends claims 1-3, 6-11, 13-14, 17-21 and 23-24. Claims 5, 16 and 22 are cancelled. Claims 30-32 are newly added. Claims 1-4, 6-15, 17-21 and 23-32 remain in the case.

The Applicant requests reconsideration.

The Applicant adds no new matter.

Amendment in the Claims

Claims 1, 13 and 20 have been amended to include features from claims 5, 16 and 22, respectively. Claims 5, 16 and 22 have been cancelled in favor of claims 1, 13 and 20 as amended hereby. Claims 7, 18 and 24 have been amended to accommodate to the amendment in claims 1, 13 and 20.

Claims 2, 14 and 20 have been amended to include a metal oxide as a material of the lower electrode. Claims 21and 23 have been amended to accommodate to the amendment in claim 20.

Claims 3, 6-11 and 17-19, which previously depend from one of independent claims, have been amended to depend from one of dependent claims, thereby narrowing the claim scope thereof.

Claim 8 have further been amended to delimit the pre-annealing range of temperatures (350°C to 499°C).

Newly added Claims

Claims 30-32 have been newly added to delimit the pre-annealing range of temperatures between 350-499°C, preferably at about 450°C. Applicant believes these claims

to be allowable over the prior art. These claims are clearly supported by last paragraph of page 6 and first paragraph of page 7 in the specification. Therefore, no new matter has been added.

Claim Rejections – 35 USC §102(e)

Claims 1-6, 8-17, 19-23 and 27 are rejected under 35 USC §102(e) as anticipated by Agarwal et al. (U.S. Pub. No. 2002/0037630). The Examiner states in paragraphs 1 and 2 of the Office Action the following, "Agarwal further teaches that the capacitor dielectric layer (28) is annealed, thus crystallized." Applicant respectfully disagrees with this statement. Instead, after careful review of the Agarwal '630 reference, Applicant can find no such specific recitation or suggestion within the reference regarding the use of a crystallized dielectric. Instead, paragraph 0048 of Agarwal '630 states only that the dielectric should have a high dielectric constant around 9, and that it be conformally formed as a "thin layer" over the enhanced surface area electrode (26) so that it preferably provides an enhanced surface area on a surface facing away from the bottom electrode. Paragraph 0055 states, in fact, that the anneal process is typically performed before the dielectric layer and second electrode are formed. And paragraph 0056 simply lists the suitable dielectric materials available.

Nothing in the Agarwal '630 reference discloses the advantages of combining the step of pre-annealing the bottom electrode of the capacitor with the step of crystallizing the dielectric. The combination of these two steps yields the unexpected experimental advantages illustrated in applicant's FIGs. 6A, 6B, 7A and 7B. Moreover, applicant respectfully point out that the purpose of the pre-annealing in the present invention is different from that of the Agarwal '630 reference. That is to say, the purpose of the pre-annealing in the present invention is to remove the impurities from the lower electrode, thereby preventing the suppression of the crystallization of the capacitor dielectric layer. Amended independent claims 1, 13, 20 and dependent claims therefrom, now incorporating the limitations of claims 5, 16 and 22, should thus be allowable over the prior art of record.

The claims have further been amended to delimit the pre-annealing range of temperatures (350°C to 499°C) to place them outside of those cited in the Agarwal reference (500°C to 900°C) with a preferred temperature of 450°C. The Examiner has stated in paragraph 3 of the Office Action that "Agarwal also teaches that the temperature required for the pre-annealing process may be reduced if reducing ambient is used." Applicant believes that the Examiner must be referring to paragraph 0035, which cites to the use of a "reducing

ambient." However, such use is clearly limited to the anneal step of the lower electrode, and not the pre-annealing step of the present invention, since the stated result of the process (see last two lines of paragraph 0035) "converts at least a portion of the ruthenium oxide to ruthenium and produces a rough surface on the layer." This is clearly at odds with the pre-anneal process where the materiality of the lower electrode does not substantially change. Accordingly, applicant respectfully requests that the Examiner's rejection of claims 6, 8, 17 and 23 be removed.

Claim Rejections – 35 USC §103

Claims 7, 18, 24 and 25 are rejected under 35 USC §103(a) as being unpatentable over Agarwal '630 in view of Aoki et al. (U.S. Patent No. 6,303,950).

Claim 26 is rejected under 35 USC §103(a) as being unpatentable over Agarwal '630.

Claims 28 and 29 are rejected under 35 USC §103(a) as being unpatentable over Agarwal '630 in view of Narwanka et al. (U.S. Patent No. 6,204,203).

As described above, all independent claims 1, 13 and 20 are believed to be in condition for allowance with the amendment thereof. Therefore, all dependent claims from the independent claims are also believed to be in condition for allowance by incorporating the limitations of the amended independent claims.

The Federal Circuit has been consistent in reversing the PTO when a rejection is made on the basis of hindsight, that is when an Examiner rejects the application under 35 U.S.C. §103(a) grounds as obvious under a combination of two or more patents without any specific suggestion within the patents to combine the features. In the case of In re Rouffett, 47 USPQ2d 1453 (Fed. Cir. 1998), the Federal Circuit refused to uphold an obviousness rejection, even where skill in the art was high, absent the specific identification of principal known to one of ordinary skill in the art that suggested the claimed combination.

The Federal Circuit reemphasized the care to be taken when combining prior art references in obviousness findings in Ecolochem v. Southern Cal. Edison, 56 USPQ2d 1065 (Fed. Cir. 2000), stating that such absence of evidence to combine prior art references "is defective as hindsight analysis." The Federal Circuit held similarly in In re Kotzab, 55 USPQ2d 1313 (Fed. Cir. 2000), reversing the PTO and stating that, "[i]dentification of prior art statements that, in abstract, appear to suggest the claimed limitation does not establish a prima facie case of obviousness without a finding as to the specific understanding or principal within the knowledge of a skilled artisan that would have motivated one with no knowledge of the invention to make the combination in the manner claimed."

Finally, the Federal Circuit has reaffirmed their view that the PTO used improper hindsight analysis to reject patent claims under §103(a) in the recent case of In re Lee, 61 USPQ2d 1430 (Fed. Cir. 2002), stating that a specific suggestion in the prior art cited is required and not "a simple citation to common knowledge and common sense."

For the foregoing reasons, reconsideration and allowance of claims 1-4, 6-15, 17-21 and 23-32 of the application as amended and newly added is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Once amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a lower electrode on a substrate;

subjecting the lower electrode to a pre-annealing, wherein the pre-annealing is a thermal annealing under a selected atmosphere;

forming a capacitor dielectric layer on the pre-annealed lower electrode, wherein the capacitor dielectric layer is formed of a crystalline material; and

forming an upper electrode on the capacitor dielectric layer.

2. (Once amended) The method of claim 1, wherein the lower electrode is formed of a material selected from the group consisting of a metal and a metal oxide.

3. (Once amended) The method of claim [1]2, wherein the lower electrode is formed by a CVD method.

Claim 5 is cancelled.

6. (Once amended) The method of claim [1]4, wherein the pre-annealing does not substantially change the materiality of the lower electrode.

7. (Once amended) The method of claim [1]4, [which further] wherein the step of forming a capacitor dielectric layer comprises [subjecting the capacitor dielectric layer to a crystallization annealing, and wherein a processing temperature of the pre-annealing is higher than that of the crystallization annealing]:

forming a capacitor dielectric layer on the pre-annealed lower electrode; and

subjecting the capacitor dielectric layer to a crystallization annealing, wherein a processing temperature of the pre-annealing is higher than that of the crystallization annealing.

8. (Once amended) The method of claim [1]6, wherein the pre-annealing is performed at a range of between [about 350 ~ 750°C] 350 ~ 499°C.

9. (Once amended) The method of claim [1]4, wherein the selected atmosphere comprises a hydrogen gas.

10. (Once amended) The method of claim [1]4, wherein the selected atmosphere comprises a nitrogen gas.

11. (Once amended) The method of claim [1]4, wherein the selected atmosphere is a mixed atmosphere.

13. (Once amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a lower electrode on a substrate;

subjecting the lower electrode to a pre-annealing, wherein the pre-annealing is a treatment exposing the lower electrode under a plasma atmosphere;

forming a capacitor dielectric layer on the pre-annealed lower electrode, wherein the capacitor dielectric layer is formed of a crystalline material; and

forming an upper electrode on the capacitor dielectric layer.

14. (Once amended) The method of claim 13, wherein the lower electrode is formed of a material selected from the group consisting of a metal and a metal oxide, and the [metal] lower electrode is formed by a CVD method.

Claim 16 is cancelled.

17. (Once amended) The method of claim [13]15, wherein the pre-annealing does not substantially change the materiality of the lower electrode.

18. (Once amended) The method of claim [13]15, [which further] wherein the step of forming a capacitor dielectric layer comprises [subjecting the capacitor dielectric layer to a crystallization annealing, and wherein a processing temperature of the pre-annealing is higher than that of the crystallization annealing]:

forming a capacitor dielectric layer on the pre-annealed lower electrode; and

subjecting the capacitor dielectric layer to a crystallization annealing, wherein a processing temperature of the pre-annealing is higher than that of the crystallization annealing.

19. (Once amended) The method of claim [13]15, wherein the plasma atmosphere comprises a hydrogen gas.

20. (Once amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a [metal] lower electrode on a substrate, wherein the [metal] lower electrode is formed by a CVD method, and wherein the lower electrode is formed of a material selected from the group consisting of a metal and a metal oxide;

subjecting the [metal] lower electrode to a pre-annealing;

forming a capacitor dielectric layer on the [metal] pre-annealed lower electrode, wherein the capacitor dielectric layer is formed of a crystalline material; and

forming an upper electrode on the capacitor dielectric layer.

21. (Once amended) The method of claim 20, wherein the pre-annealing is one selected from the group consisting of a thermal annealing under a selected atmosphere and a treatment exposing the [metal] lower electrode under a plasma atmosphere.

Claim 22 is cancelled.

23. (Once amended) The method of claim 21, wherein the pre-annealing does not substantially change the materiality of the [metal] lower electrode.

24. (Once amended) The method of claim 21, [which further] wherein the step of forming a capacitor dielectric layer comprises [subjecting the capacitor dielectric layer to a crystallization annealing, and wherein a processing temperature of thermal annealing is higher than that of the crystallization annealing]:

forming a capacitor dielectric layer on the pre-annealed lower electrode; and

subjecting the capacitor dielectric layer to a crystallization annealing, wherein a processing temperature of the pre-annealing is higher than that of the crystallization annealing.

Claims 30-32 are new.